CLAIMS

What is claimed is:

1. A memory management circuit for managing a memory having a plurality of memory blocks, each memory block having a plurality of memory segments, the memory management circuit comprising:

a first logic circuit associated with a first memory block of the plurality of memory blocks, the first logic circuit having a first state when the first memory block has a memory segment that is available for data storage and a second state when the first memory block does not have a memory segment that is available for data storage.

2. The memory management circuit of claim 1, further comprising a second logic circuit associated with a first memory segment of the first memory block, the second logic circuit having a first state when the first memory segment is available for data storage and a second state when the first memory segment is not available for data storage.

3. The memory management circuit of claim 1, wherein the first state and second state are states of a single logic bit.

4. The memory management circuit of claim 1, wherein the first state includes at least a portion of a memory address of the first memory block.

5. The memory management circuit of claim 1, further comprising a second logic circuit having a plurality of logic sub-circuits, each logic sub-circuit corresponding to a respective one of the memory segments of the first memory block, each logic sub-circuit having a first state when its respective memory segment is available for data storage and a second state when its respective memory segment is not available for data storage.

6. The memory management circuit of claim 2, further comprising a third logic circuit having a state indicative of a memory address of the first memory segment.

7. The memory management circuit of claim 2, further comprising a third logic circuit that converts the first state of the first logic circuit and the first state of the second logic circuit to the memory address of the first memory segment.

8. The memory management circuit of claim 2, wherein the first and second states of the first logic circuit are states of a single logic bit and the first and second states of the second logic circuit are states of a single digital bit.

9. The memory management circuit of claim 2, wherein the first state of the first logic circuit is indicative of a memory address of the first memory block and the first state of the second logic circuit is indicative of a memory offset between the memory address of the first memory block and the memory address of the first memory segment.

10. A memory management circuit for managing a memory having a first and second memory block, each memory block having a first and second memory segment, the memory management circuit comprising:

a first logic circuit having a first state when any of the memory segments of the first memory block are available for data storage and a second state when none of the memory segments of the first memory block are available for storage; and

a second logic circuit having a first state when any of the memory segments of the second memory block are available for data storage and a second state when none of the memory segments of the second memory block are available for data storage.

11. The memory management circuit of claim 10, further comprising:

a third logic circuit having a first state when the first memory segment of the first memory block is available for data storage and a second state when the first memory segment of the first memory block is not available for data storage; and

a fourth logic circuit having a first state when the second memory segment of the first memory block is available for data storage and a second state when the second memory segment of the first memory block is not available for data storage.

12. The memory management circuit of claim 11, further comprising:

a fifth logic circuit having a first state when the first memory segment of the second memory block is available for data storage and a second state when the first memory segment of the second memory block is not available for data storage; and

a sixth logic circuit having a first state when the second memory segment of the second memory block is available for data storage and a second state when the second memory segment of the second memory block is not available for data storage.

13. A memory management system for managing a memory having a plurality of memory blocks, each memory block having a plurality of memory segments, the memory management system comprising:

a first bitmap having a sequence of bits, each bit of the first bitmap corresponding to a respective one of the plurality of memory blocks, each bit of the first bitmap having a first logic state if the bit's respective memory block has a memory segment that is available for data storage and a second logic state if the bit's respective memory block does not have a memory segment that is available for data storage; and

a second bitmap having a sequence of bits, each bit of the second bitmap corresponding to a respective one of the plurality of memory segments of the memory, each bit of the second bitmap having a first logic state if the bit's respective memory segment is available for data storage and a second logic state if the bit's respective memory segment is not available for data storage.

14. The memory management system of claim 13, further comprising a logic circuit that identifies a bit in the first bitmap having the first logic state.

15. The memory management system of claim 13, further comprising a logic circuit that identifies a memory block having a memory segment available for data storage by identifying a first bit in the first bitmap having a state indicative of the first bit's respective memory block having a memory segment available for data storage, and identifies a memory segment that is available for data storage by identifying a second bit in the second bitmap having a logic state indicative of the second bit's respective memory segment being available for data storage.

16. The memory management system of claim 15, wherein the logic circuit identifies the second bit in the second bitmap by analyzing only bits in the second bit map that correspond to memory segments in the identified memory block.

17. The memory management system of claim 15, wherein the logic circuit determines the address of the memory segment that is available for data storage by generating a most significant portion of the address according to the position of the first bit in the first bitmap sequence of bits, and generating a least significant portion of the address according to the position of the second bit in the second bitmap sequence of bits.

18. The memory management system of claim 13, further comprising a logic circuit that identifies a bit in the second bitmap corresponding to a memory segment that is available for data storage based on a least significant portion of the address of the memory segment, and sets the logic state of the identified bit in the second bitmap to indicate that the memory segment is available for data storage.

19. The memory management system of claim 18, wherein the logic circuit further identifies a bit in the first bitmap corresponding to a memory block that includes the memory

segment based on a most significant portion of the address of the memory segment, and sets the logic state of the identified bit in the first bitmap to indicate that the memory block includes a memory segment that is available for data storage.

20. The memory management system of claim 13, further comprising a logic circuit that converts a most significant portion of a memory segment address to a bit position in the first bitmap sequence of bits.

21. The memory management system of claim 13, further comprising a logic circuit that converts a most significant portion of a memory segment address to a bit position in the first bitmap sequence of bits, and sets the bit located at the bit position in the first bitmap to a logic state indicative of the bit's respective memory block having at least one memory segment available for data storage.

22. The memory management system of claim 13, further comprising a logic circuit that converts a least significant portion of a memory segment address into a bit position in the second bitmap sequence of bits.

23. The memory management system of claim 13, further comprising a logic circuit that converts a least significant portion of a memory segment address into a bit position in the second bit map sequence of bits, and sets the bit located at the bit position in the second bit map to a logic state indicative of the bit's respective memory segment being available for data storage.

24. A method for managing memory, the method comprising:

analyzing a first flag to determine whether a block of memory segments includes a memory segment that is available for data storage; and

if the block of memory segments includes a memory segment that is available for data storage, identifying a memory segment in the block of memory segments that is available for data storage.

25. The method of claim 24, wherein identifying a memory segment in the block of memory segments that is available for data storage comprises analyzing a second flag to determine whether a particular memory segment in the block of memory segments is available for data storage.

26. The method of claim 24, wherein identifying a memory segment in the block of memory segments that is available for data storage comprises:

analyzing a second flag to determine whether a first memory segment in the block of memory segments is available for data storage;

if the first memory segment in the block of memory segments is available for data storage, determining the address of the first memory segment; and

if the first memory segment in the block of memory segments is not available for data storage, analyzing a third flag to determine whether a second memory segment in the block of memory segments is available for data storage.

27. The method of claim 26, wherein the first flag is a flag in an array of flags, and determining the address of the first memory segment comprises converting a position of the first flag in the array of flags to a most significant portion of the address of the first memory segment.

28. The method of claim 26, wherein the second flag is a flag in an array of flags, and determining the address of the first memory segment comprises converting a position of the second flag in the array of flags to a least significant portion of the address of the first memory segment.

29. The method of claim 26, wherein the second flag is a flag in an array of flags, and determining the address of the first memory segment comprises converting a position of the second flag in the array of flags to the address of the first memory segment.

30. The method of claim 24, wherein identifying a memory segment in the block of memory segments that is available for data storage comprises analyzing a set of flags, each flag corresponding to a respective memory segment in the block of memory segments, to identify a memory segment in the block of memory segments that is available for data storage.

31. The method of claim 24, further comprising:

if the block of memory segments does not include a memory segment that is available for data storage, analyzing a second flag to determine whether a second block of memory segments includes a memory segment that is available for data storage; and

if the second block of memory segments includes a memory segment that is available for data storage, identifying a memory segment in the second block of memory segments that is available for data storage.

32. A method for managing a memory, the memory having a plurality of memory blocks, each of the plurality of memory blocks having a plurality of memory segments, the method comprising:

representing each of the plurality of memory blocks with a respective bit in a first bitmap, the logic state of each respective bit in the first bitmap indicative of whether each bit's respective memory block has at least one memory segment that is available for data storage; and

representing each of the memory segments with a respective bit in a second bitmap, the logic state of each respective bit in the second bitmap indicative of whether each bit's respective memory segment is available for data storage.

33. The method of claim 32, further comprising identifying a memory block that has a memory segment available for data storage by locating a bit in the first bitmap that has a logic state indicative of the memory block having a memory segment available for data storage.

34. The method of claim 33, further comprising identifying a memory segment that is available for data storage by locating a bit in the second bitmap that has a logic state indicative of the memory segment being available for data storage.

35. The method of claim 34, wherein locating a bit in the second bitmap that has a logic state indicative of the memory segment being available for data storage comprises:

identifying the position of the bit in the first bitmap that corresponds to the identified memory block;

utilizing the position of the bit in the first bitmap to index to a location in the second bitmap at which the bits corresponding to the memory segments in the identified memory block are located; and

analyzing at least one of the bits corresponding to the memory segments in the identified memory block to identify a bit that has a logic state indicative of the bit's respective memory segment being available for data storage.

36. The method of claim 34, further comprising determining the memory address of the memory segment available for data storage by converting the position of the bit in the first bitmap to a most significant portion of the memory address, and converting the position of the bit in the second bitmap to a least significant portion of the memory address.

37. The method of claim 32, further comprising designating that a memory segment is available for data storage by determining a position of a bit in the first bitmap that corresponds to a memory block that includes the memory segment, and setting the bit in the

first bitmap to a logic state indicative of the memory block having a memory segment available for data storage.

38. The method of claim 32, further comprising designating that a memory segment is available for data storage by determining a position of a bit in the second bitmap that corresponds to the memory segment, and setting the bit in the second bitmap to a logic state indicative of the memory segment being available for data storage.

39. The method of claim 37, further comprising designating that a memory segment is available for data storage by determining a position of a bit in the second bitmap that corresponds to the memory segment, and setting the bit in the second bitmap to a logic state indicative of the memory segment being available for data storage.

40. The method of claim 37, wherein determining a position of a bit in the first bitmap comprises converting a most significant portion of the memory address of the memory segment into the position of the bit in the first bitmap.